

# Hardware Based Flash Memory Failure Characterization Platform

## Abstract

The use of Flash memory is rapidly expanding worldwide due to a decrease in manufacturing costs and an increase in memory density and capacity. Manufactures guarantee that SLC NAND Flash memory will operate for up to 100,000 Program-and-Erase cycles, but failure rates beyond this point are usually unavailable since they will vary significantly between manufactures and product lines. This paper will discuss the development of an open source testing platform for analyzing Flash failure rates beyond the manufactures guaranteed lifetime and will present our initial research findings. The goal is to provide a low cost and easy to use test platform that product engineers can use to evaluate the life expectancy of Flash memory under specific use patterns to improve the use of Flash technology in future devices.

## Outline

1. Introduction: background, project goals, and intended use
2. Hardware testing platform
  - a) Interactive C# based GUI on host PC for creating Flash test scripts, collecting failure results in MS SQL database, and analyzing failure data.
  - b) Altera DE2 FPGA using modular System-On-A-Programmable-Chip (SOPC) architecture to interface with GUI and Flash controller.
  - c) Verilog based Flash controller quickly executes commands on Flash device and returns results to C based firmware for processing.
  - d) Flash daughter card interface for FPGA (48 Pin TSOP Type 1 socket)
3. Project demonstration and results: live demo and presentation of testing results for over 100,000 Program/Erase cycles

## Biography

The Flash testing platform was designed by a team of 5 students from the University of Utah Electrical and Computer Engineering (ECE) department as part of the 2007-2008 senior engineering clinic that was sponsored by the Micron Foundation. The team members were Greg Bray (Team Lead, BS Computer Engineering), Kyle Stewart (Technical Lead, BS Computer Engineering), Jeffrey Gorton (Documentation Lead, BS Electrical Engineering), Jonathan Morgan (Data Analyst, BS Electrical Engineering) and Garrett Thomas (Quality Assurance, BS Electrical Engineering). Ken Stevens was the faculty advisor, and Dennis Zattiero and Dean Klein provided assistance from the Micron Foundation. More information regarding the project can be found online at:

<http://code.google.com/p/2007-uofu-micron-clinic/>